Customer No.:31561
Application No.: 10/709,372
Docket NO.: 12409-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1-6 and 9-10 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. 6,486,028; hereafter Chang) in view of Fastow et al. (U.S. 6,583,479; hereafter Fastow). The Office Action also rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Fastow and further in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes). Applicant deems that claims 1-10 have already clearly defined the invention and been distinguishable over the cited arts. Hence, the reconsideration of those claims is respectfully requested.

Summary of Applicants' Invention

The Applicants' invention is directed to a non-volatile memory cell with a gate, a first source/drain region, a second source/drain region and a third source/drain region. The gate is located in a trench within a substrate, the first source/drain region (206) is located in the substrate under the bottom of the gate, the second source/drain region is located at one side of the gate in the substrate and the third source/drain region is located at the other side of the gate in the substrate. Since the second source/drain region and the third source/drain region are electrically connected to **the same common bit line**, **a single non-volatile memory cell can be regarded as two transistor connected in parallel**. That is, a first transistor, which is composed of the first source/drain region (206), the second source/drain region and the gate (208), and a second transistor, which is composed of the first source/drain region (206), the third source/drain region and the gate

(208) are connected in parallel. In this dual transistor structure, the gates of the transistors are electrically connected to a common word line, **the sources are electrically connected to the same common source line** and **the drains are electrically connected to the same common bit line** (as shown in Fig. 3 and paragraph [0036]). Hence, with this configuration, the density of current flowing through the non-volatile memory cell is increased and the efficiency of programming/erasing operation is improved.

Telephonic Interview with Examiner

The undersigned would like to thank Examiner Tran for granting a telephonic interview on the July 11, 2005, during which the 103(a) rejection in the Office Action dated 5/20/2005 was discussed. More particularly, the undersigned and the Examiner discussed the obvious rejection and the teachings of Fastow. The undersigned clarified to the Examiner that the second and third S/D regions 214 of the present invention, on each side of the gate respectively, are connected to a same bit line 220 through plugs 218 as shown in Figure 2B, whereas the alleged second and third S/D regions of Fastow are connected to separate bit lines 826. Examiner Tran acknowledged our point and recommended that we file a written response for further reconsideration and search.

Discussion of Office Action Rejections

The Office Action rejected claims 1-6 and 9-10 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. 6,486,028; hereafter Chang) in view of Fastow et al. (U.S. 6,583,479; hereafter Fastow).

Applicants respectfully traverse this rejection and submit that Chang in view of Fastow is legally deficient to render claims 1-6 and 9-10 unpatentable. As stated, claim 1 recites:

> Claim 1. A non-volatile memory cell, comprising:
> a substrate, having a trench thereon;
> a gate, formed within the trench;
> a first source/drain region, formed at a bottom of the trench;
> a composite dielectric layer, formed between the gate and a surface of the trench, wherein the composite dielectric layer comprises at least a charge-trapping layer;
> a second source/drain region, formed in the substrate on one side of the gate; and
> a third source/drain region located in the substrate on the other side of the gate, wherein **the second source/drain region and the third source/drain region are electrically connected to a common bit line.**

(***Emphasis added***). Applicants submit that claim 1 patently defines over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

In the present invention, **the second source/drain region** located at one side of the gate 208 (as shown in 2B) and **the third source/drain region** located at the other side of the gate 208 **are electrically connected to the same common bit line** in order to increase the density of the current flowing through the non-volatile memory cell so as to improve the efficiency of programming/erasing operation (as shown in Fig. 3 and paragraph [0036]).

However, Chang fails to teach or suggest that the first source/drain region 104 and the second source/drain region 106 (as shown in Fig. 6 in the cited art) are electrically connected to the same common bit line.

The Office Action stated that although Change does not disclose that the second

source/drain and the third source/drain region are electrically connected to a common bit line, Fastow, in Fig. 10, teaches the issues mentioned above. Applicants respectfully traverse this indication and would like to attract Examiner's attention on Fig. 10 of Fastow's application. In Fig. 10 and col. 14, lines 36-38, Fastow shows that sources of the cells 822 and 824 are connected to a contact 820 and, however, **the drains of cells 822 and 824 are connected to the different contacts 826 respectively**. Fastow fails to teach or suggest that the drains of cells 822 and 824 are electrically connected to **the same contact 826**.

Hence, even the skilled artisan modified Chang's application by referring to Fastow's application, the combination result would not possesses the same advantage as what claimed in the present invention.

Therefore, Applicants respectfully submit that Chang in view of Fastow fails to render claim 1 unpatentable. Claims 2-6 and 9-10, which depend from claim 1, are also patentable over Chang in view of Fastow, at least because of their dependency from an allowable base claim. Applicants respectfully assert that these claims are in condition for allowance. Thus, reconsideration and withdrawal of this rejection are respectively requested.

The Office Action also rejected claims 7 and 8 under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Fastow and further in view of Forbes (U.S. pub. No. 2003/0235076; hereafter Forbes).

Since claims 7 and 8 are dependent claims which further define the invention

recited in claim 1, Applicants respectfully assert that these claims also are in condition for allowance according to the same reasons as discussed above for the rejection 103. Thus, reconsideration and withdrawal of this rejection are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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